In the Claims:

Please replace all previous claim listings with the following claim listing:

1. (Currently Amended) A semiconductor device ~~test pattern~~, comprising:

(a) a test pattern that includes

a word line on a semiconductor substrate;

an active region comprising a first impurity doped region and a second impurity doped region;

a first ~~self-aligned~~ contact pad electrically connected to the first impurity doped region, the first contact pad having a first region that covers the first impurity doped region and a second region that is offset from the first impurity doped region;

a first bit line electrically connected to the first ~~self-aligned~~ contact pad;

~~a first probing pad electrically connected to the first bit line;~~

a second ~~self-aligned~~ contact pad electrically connected to the second impurity doped region;

a second conductive line electrically connected to the second ~~self-aligned~~ contact pad; and

(b) a first probing pad electrically connected to the first bit line; and

(c) a second probing pad electrically connected to the second conductive line.

2. (Currently Amended) The semiconductor device ~~test pattern~~ of Claim 1, further comprising:

~~a first direct contact electrically connected to the first self-aligned contact pad~~

a first contact plug that penetrates a first insulation layer between the first contact pad and the first bit line, the first contact plug electrically connecting the first contact pad to the first bit line; and

~~a second contact electrically connected to the second self-aligned contact pad~~

a second contact plug that penetrates the first insulation layer, the second contact plug electrically connecting the second contact pad to the second conductive line.~~;~~

3. (Currently Amended) The semiconductor device ~~test pattern~~ of Claim 1, wherein the first ~~self-aligned~~ contact pad is one of a plurality of discrete first ~~self-aligned~~ contact pads disposed between the word line and a second word line.

4. (Currently Amended) The semiconductor device ~~test pattern~~ of Claim ~~1,~~ 3, further comprising an insulating pattern that electrically insulates each of the plurality ~~disposed between each~~ of the discrete first ~~self-aligned~~ contact pads from one another. ~~disposed between the word line and a second word line.~~

5. (Currently Amended) The semiconductor device ~~test pattern~~ of Claim 1, further comprising a ~~first metal~~ third contact plug between the first bit line and the first probing pad that electrically connects the first bit line and the first probing pad.

6. (Currently Amended) The semiconductor device ~~test pattern~~ of Claim 1, further comprising a ~~second metal~~ fourth contact plug between the second conductive line and the second probing pad that electrically connects the second conductive line and the second probing pad.

7. (Currently Amended) The semiconductor device ~~test pattern~~ of Claim 1, wherein the second impurity doped region is one of a plurality of second doped impurity regions disposed between the word line and a second word line, and wherein the second ~~self-aligned~~ contact pad extends in a continuous line between the word line and the second word line to electrically connect to the plurality of second impurity doped regions.

8. (Currently Amended--Withdrawn) The semiconductor device ~~test pattern~~ of Claim 1, wherein the first bit line is perpendicular to a major axis of the active region.

9. (Currently Amended) The semiconductor device ~~test pattern~~ of Claim 1, wherein the second conductive line ~~is a second bit line that~~ is perpendicular to the word line.

10. (Currently Amended--Withdrawn) The semiconductor device ~~test pattern~~ of Claim 2, wherein the second contact plug is a buried contact.

11. (Currently Amended--Withdrawn) The semiconductor device ~~test pattern~~ of Claim 1, wherein a major axis of the active region is at an oblique angle with respect to the word line.

12. (Currently Amended--Withdrawn) The semiconductor device ~~test pattern~~ of Claim 1, wherein the second conductive line ~~is a second bit line that~~ is parallel to the word line.

13. (Currently Amended--Withdrawn) The semiconductor device ~~test pattern~~ of Claim 1, wherein the first bit line and the second conductive line have a plurality of arms, and wherein one of the arms of the first bit line is disposed between each adjacent set of arms of the second conductive line.

14. (Currently Amended--Withdrawn) The semiconductor device ~~test pattern~~ of Claim 1, wherein the second ~~self-aligned~~ contact pad is one of a plurality of discrete second ~~self-aligned~~ contact pads disposed between the word line and a second word line.

15. (Currently Amended--Withdrawn) The semiconductor device ~~test pattern~~ of Claim 14 ~~13~~, wherein the second impurity doped region is one of a plurality of discrete second impurity doped regions disposed between the word line and the second word line, and wherein each of the second ~~self-aligned~~ contact pads electrically connects to two of the discrete second impurity doped regions.

16. (Currently Amended--Withdrawn) The semiconductor device ~~test pattern~~ of Claim 3, wherein the second ~~self-aligned~~ contact pad is one of a plurality of discrete second ~~self-aligned~~ contact pads disposed between the word line and a second word line, and wherein the one of the plurality of second ~~self-aligned~~ contact pads is disposed between adjacent of the first ~~self-aligned~~ contact pads.

17-42. (Cancelled)

43. (New) The semiconductor device of Claim 1, wherein the first bit line is laterally offset from the first and second impurity doped regions.

44. (New) The semiconductor device of Claim 5, further comprising a second insulating layer between the first bit line and the first probing pad, wherein the third contact plug penetrates the insulating layer.

45. (New) The semiconductor device of Claim 5, further comprising a second insulating layer between the second conductive line and the second probing pad, wherein the fourth contact plug penetrates the insulating layer.

46. (New) The semiconductor device of Claim 1, wherein the first bit line is over the second region of the first contact pad.